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10/612,193	07/03/2003	Takashi Takenaka	043034-0180	4129

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,193	TAKENAKA, TAKASHI	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been presented for examination.

Response to Arguments

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 20 August 2007 has been entered.

i) Applicant's arguments filed 20 August 2007 have been fully considered but they are not persuasive.

ii) Applicants argue the 101 rejections of the claims. Applicant argues that the recitation of the means for determining produces a useful concrete and tangible result. As per the output device recited in the steps in conjunction with determination the 101 rejections of claims 1-11 and 21 are withdrawn. However claims 12-20 do not recite means for and therefore the limitations from the specification cannot be brought into the claims therefore the rejection is maintained for claims 12-20. The Examiner has explained previously the rationale for the rejection and reproduces it below. The mere comparison of cones does not produce a useful concrete and tangible result since at the very least the mere comparison of cones does not produce a tangible or concrete result.

iii) Applicant argues the 112 2nd rejection of the claims. First Applicants have stated that one of ordinary skill in the art would readily understand in view of the specification how a determination is made. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., how the determination is made) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore the rejection is maintained. With respect to Applicant statement that the means plus function nature of the claims overcomes this rejection the Examiner notes that claims 12-20 do not recite means plus function and further that the specification. Further Applicants state that claim 2 recites "one way" a determination can be made. This statement reinforces the Examiners position in that the claims do not explicitly recite how a determination is made. The statement that "one way" a determination can be made does not result in an explicit definition. Therefore the

rejection is maintained. Finally, the term acceptable is still rejected by the Examiner since the term is vague an indefinite and Applicants have yet to provide any specificity with respect to this term in the claim language as presented.

iv) Applicants argue that the Office action does not provide an element-by-element listing of where a particular claim element is taught in the cited art. First, the Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, **to fully consider the references in their entirety as potentially teaching all or part of the claimed invention,** as well as the context of the passage as taught by the prior art or disclosed by the Examiner. The Examiner notes that an element-by-element listing is not a requirement and citations of the references are for the convenience of the Applicant, however the Examiner has reproduced the references citations below in a more categorized manner with further reference interpretation for further convenience to the Applicant. The Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as **limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed** ***by explaining the differences between Applicants claimed invention and the prior art presented.***

v) Applicant's arguments once again fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Further, Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

It is noted that Applicant has merely summarized the Foster reference based on a single section and then states that the reference does not teach based on Foster not being "pertinent to the presently claimed invention." Applicants then state, "Blackett and Lu suffer similar deficiencies."

Applicant then relies on an interpretation of the specification to overcome the rejection by citing several sections of the specification of the instant application. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., how the determination is made) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

vi) Applicants state:

> Foster, Blackett and Lu merely describe a technique for verifying "the behavioral level description 12", and not a technique for verifying that the "object code 15" is equivalent to the RT level description 14." Please note that "object code" is recited in each of the presently pending independent claims, whereby the use of the object code in the manner claimed in not disclosed or suggested by Foster, Blackett and Lu.

First the Examiner notes that Applicants have provided no specific arguments, for example by citing either Blackett or Lu, with respect to the Blackett and Lu references and has merely summarized a single section of Foster. Second, the claims of the present invention state that the object code is compiled from an behavioral level description. Applicants then state that the references teach a behavioral level description but not an equivalency determination. As cited previously,

Foster, as cited in the previous office action, on Page 12, "Effective equivalence checking methodology and Early Often" recites "RTL-to-gate" and "gate-to-gate" comparison for designs.

Blackett, as cited in the previous office action, on Page 70, Paragraph 1, and "Equivalence checking in use," recites comparison and RTL design equivalence checking. See also Figure 1, which is a logic cone.

Lu, as cited in the previous office action, on Page 8, Paragraph 3, recites equivalence checking and logic cones.

vii) Applicants state:

In more detail, Foster, Blackett and Lu describe features that are similar to the prior art described on pages 5 of the specification ("JP8-22485 and Edmund Clarke et al., "Model Checking") and pages 10 and 11 of the specification ("International Conference on Computer Design, pp. 458-466, 1999").

The Examiner is puzzled by this assertion since Applicants have repeatedly argued that the references do not teach Applicants invention by citing certain sections of the specification of the instant application and here state that the references do teach features similar to those found in the specification of the instant application. Applicants are respectfully requested to clarify their arguments with respect to the prior art, **in its entirety,** and further **in view of the claims as recited.** Applicants are further respectfully requested to indicate where the 112 6th paragraph is intended to be invoked in order to avoid further confusion similar to this cited section of Applicants remarks.

viii) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

PRIORITY

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

4. **Claims 12-20 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) The claims recite a system, method, and computer program. It should be noted that the claims do not appear to produce a useful, concrete, and tangible result since the claims are directed to merely a comparison of cones. Further, Applicants have not demonstrated how the claims produce a useful, concrete, and tangible result since the claims still recite, in their broadest reasonable interpretation, a comparison of cones.

ii) The claims contain numerous instances of intended use, which are outlined below.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 1-21 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i) Applicants amendment recites a determination is made as to whether logic circuits that have been designed... are acceptable to be used. First, it is unclear how a determination is made. Merely stating comparison does not indicate how the comparison is made or what is being compared. Second, it is unclear as to what qualifies as acceptable. Is there an acceptable threshold? Third, it is unclear what mechanism is used to determine acceptability. This renders the claims incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: mechanism to determine acceptability, threshold of comparison, type of comparison, and mechanism for comparison. Fourth, the claim limitations contain numerous intended use statements. These issues render the claims vague and indefinite.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-20 are rejected** under 35 U.S.C. 102(a) as being clearly anticipated by **"Applied Boolean Equivalence Verification and RTL Static Sign-Off", Harry Foster, hereafter referred to as Foster.**

7. **Claims 1-20 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **"As good as gold", Blackett, hereafter referred to as Blackett.**

8. **Claims 1-20 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **"On the Formal Verification of ATM Switches", Jianping Lu, hereafter referred to as Lu.**

Claim Interpretation. It is noted that the phrases "used to", "used for", "to be used in", "for extracting", "for comparing", "for storing", "for compiling", "for receiving", etc. represent an intended use and are therefore not afforded patentable weight.

Regarding Claim 1:

The references disclose A logic verification system comprising:

a first logic cone extraction section for extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

wherein means for determining based on the logic cones, whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 2:

The references disclose The logic verification system according to claim 1, further comprising:

a second logic cone extraction section for extracting second logic cones from an RT level description;

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

and a logic cone comparison section for comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones;

wherein based on the comparison of the first logic cones and the second logic cones, the determining means determines whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 3:

The references disclose The logic verification system according to claim 1, wherein the first logic cone extraction section includes a symbolic simulation section.

((Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 4:

The references disclose The logic verification system according to claim 2, wherein the first logic cone extraction section includes a symbolic simulation section.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 5:

The references disclose A logic verification system comprising:

a storage section for storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase,

an RT level description generated from the behavioral level description,

correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair,

and compile information including mapping information between the behavioral level description and the object code;

(The citations below discuss equivalency checking as well as model descriptions)

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

a first logic cone extraction section for extracting first logic cones of variables by

searching a code portion and the variables of the object code corresponding to each fragments of descriptions and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information,

setting initial symbol values in the variables,

performing symbolic simulation from the start to end points of the code portion to produce symbol values when the variable symbolic simulation ends,

and using the symbol values as the first logic cones of the variables;

a second logic cone extraction section for extracting second logic cones each for the signals for each fragments of description of RT level description to be compared which are specified by the correspondence information;

a logic cone comparison section for comparing the first logic cones and the second logic cones for each signals for each of the fragments of descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information;

(The citations below discuss logic cones, as well as equivalency checking)

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

means for determining based on the comparison of the first logic cones and the second logic cones, whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 6:

The references disclose A logic verification system comprising:

a first logic cone extraction section for extracting first logic cones from a machine-executable object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

a storage section for storing properties to be met by the behavioral level description;

(The citations below discuss logic cones, as well as equivalency checking)

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

and a model checking section for checking whether the object code meets the properties,

means for determining based on the logic cones, whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits.

(The citations below discuss equivalency checking as well as model descriptions)

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 7:

The references disclose A logic cone extraction apparatus comprising:

an input section for inputting an object code compiled from a program description, correspondence information which specifies logic cone extraction areas within the program description and signals to be extracted

for each of the logic cone extraction areas, and compile information including mapping information between the program description and the object code, the object code being used for specification verification by simulation on a CPU in a design phase;

a symbolic simulation section which, by referencing the compile information, searches a code portion and variables of the object code corresponding to logic cone extraction areas and signals to be extracted which are specified by the correspondence information, sets initial symbol values in the variables, and performs symbolic simulation from the start to end points of the code portion;

an output section for outputting symbol values which are obtained when the variable symbolic simulation ends, as logic cones of the variables.

(The citations below discuss logic cones, as well as equivalency checking)

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

means for determining based on the logic cones of the variables, whether logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(The citations below discuss equivalency checking as well as model descriptions)

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 8:

The references disclose A logic verification method comprising the step of extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase,

Means for determining, whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 9:

The references disclose The logic verification method according to claim 8, further comprising the steps of:

extracting second logic cones from an RT level description;

and comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones,

(The citations below discuss logic cones, as well as equivalency checking)

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

wherein based on the comparison of the first logic cones and the second logic cones, a determination is made as to whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 10:

The references disclose The logic verification method according to claim 8, wherein the first logic cones are extracted by performing symbolic simulation.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 11

The references disclose The logic verification method according to claim 9, wherein the first logic cones are extracted by performing symbolic simulation.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 12

The references disclose A logic verification method comprising the steps of:

inputting an object code compiled from an behavioral level description written in a programming language, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and compile information including mapping information between the behavioral level description and the object code, the object code being used for specification verification by simulation on a CPU in a design phase;

searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison.)

(Lu, Page 102, First paragraph, RTL, Behavioral equivalency checking)

(Blackett, Page 69, Left Column, RTL and gate level information)

setting initial symbol values in the variables;

performing symbolic simulation from the start to end points of the code portion;

determining first logic cones of the variables as symbol values when the variable symbolic simulation ends;

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2.)

(Lu, Page 13, Symbolic Model Verifier)

(Blackett, Page 69, Left Column, symbolic signals and logic cones)

extracting second logic cones each for the signals for each fragments of RT level description to be compared which are specified by the correspondence information;

and comparing the first logic cones and the second logic cones for each signals for each of the descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information; and

determining, based on the comparing step, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 13

Foster discloses A logic verification method comprising the steps of:

extracting first logic cones from a machine-executable object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

inputting properties to be met by the behavioral level description;

checking whether the object code meets the properties, and

determining based on the logic cones, whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(See rejection for claims 1, 5, and 12)

Regarding Claim 14

The references disclose A logic cone extraction method comprising the steps of:

inputting an object code compiled from a program description, correspondence information which specifies logic cone extraction areas within the program description and signals to be extracted for each of the logic cone extraction areas, and compile information including mapping information between the program description and the object code, the object code being used for specification verification by simulation on a CPU in a design phase;

searching a code portion and variables of the object code corresponding to logic cone extraction areas and signals to be extracted which are specified by the correspondence information by referencing the compile information;

setting initial symbol values in the variables;

performing symbolic simulation from the start to end points of the code portion;

and outputting symbol values which are obtained when the variable symbolic simulation ends, as logic cones of the variables;

determining based on the logic cones, whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(See rejection for claims 1, 5, and 12)

Regarding Claim 15

The references disclose A computer program product embodied in computer readable medium and comprising code that, when executed causes a computer to perform logic verification, the program product comprising the steps of:

a) extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

b) extracting second logic cones from an RT level description; and

c) comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones.

d) determining, based on the comparison of the first logic cones and the second logic cones, a determination is made as to whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(See rejection for claims 1, 5, and 12)

Regarding Claim 16

The references disclose The computer program product according to claim 15, wherein, in the step a), the first logic cones are extracted by performing symbolic simulation.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 17

The references disclose A computer program product embodied in a computer readable medium and comprising code that, when executed, causes a computer to perform logic verification, the program product comprising the steps of:

a) storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and compile information including mapping information between the behavioral level description and the object code;

b) extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language;

c) extracting second logic cones from an RT level description;

d) comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones; and

e) determining, based on the comparison of the first logic cones and the second logic cones, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable in a manufacturing phase for the logic circuits,

wherein the step b) comprises the steps of:

b.1) searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

b.2) setting initial symbol values in the variables;

b.3) performing symbolic simulation from the start to end points of the code portion;

and b.4) determining the first logic cones of the variables as symbol values when the variable symbolic simulation ends.

(See rejection for claims 1, 5, and 12)

Regarding Claim 18

The references disclose The computer program product according to claim 17, wherein

the step b) comprises the step of extracting the second logic cones each for the signals for each fragments of RT level description to be compared which are specified by the correspondence information,

and the step c) comprises the step of comparing the first logic cones and the second logic cones for each signals for each of the fragments of descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 19

The references disclose A computer program product embodied in a computer readable medium and comprising code that, when executed, causes a computer to perform logic verification, the program product comprising the steps of:

extracting first logic cones from a machine-executable object code compiled from an behavioral level description written in a programming language;

inputting properties to be met by the behavioral level description;

and checking whether the object code meets the properties based on the first logic cones.

determining whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(See rejection for claims 1, 5, and 12)

Regarding Claim 20

The references disclose A computer program product embodied in a computer readable medium and comprising code that, when executed, causes a computer to perform logic cone extraction, the logic cone extraction comprising the steps of:

inputting an object code compiled from a program description, correspondence information which specifies logic cone extraction areas within the program description and signals to be extracted for each of the logic cone

extraction areas, and compile information including mapping information between the program description and the object code, the object code being used for specification verification by simulation on a CPU in a design phase;

searching a code portion and variables of the object code corresponding to logic cone extraction areas and signals to be extracted which are specified by the correspondence information by referencing the compile information;

setting initial symbol values in the variables;

performing symbolic simulation from the start to end points of the code portion;

and outputting symbol values which are obtained when the variable symbolic simulation ends, as logic cones of the variables,

determining, based on the symbol values, whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(See rejection for claims 1, 5, and 12)

Regarding Claim 21

The references disclose A logic cone extraction apparatus comprising:

a first storage section for storing correspondence information which species logic cone extraction areas within a program;

a first data processing device for compiling an object code from a program description, the object code being used to describe logic circuits in a design phase for the logic circuits;

a second storage section for storing the compiled object code output by the first data processing device, and compile information;

a second data processing device for receiving program code describing logic cones, and for receiving the complied object code and the compile information stored in the second storage section, the second data processing device computing and outputting behavioral level logic cones and RT level logic cones;

and a third storage section for storing the behavioral level logic cones .and RT level logic cones output by the second data processing device;

and a third data processing device for receiving the behavioral level logic cones and the RT level logic cones stored in the third storage section, the correspondence information stored in the first storage section, and the compile information stored in the second storage section, and for performing logic cone comparisons as a result thereof, and

determining means for determining, based on the comparisons of the logic cones performed by the third data processing device, whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(See rejection for claims 1, 5, and 12)

Conclusion

9. All Claims are rejected.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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SAA

October 20, 2007

KAMINI SHAH
SUPERVISORY PATENT EXAMINER